ADVANCED MATERIALS

A Three-Dimensional Porous Silicon p–n Diode for Betavoltaics and Photovoltaics**

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Modern society is experiencing an ever-increasing demand for energy to power a vast array of electrical and mechanical devices. As hydrocarbon resources dwindle, utilization of ample nuclear energy and abundant solar energy becomes more and more attractive. For 50 years, since the invention of the transistor, semiconductor devices that convert the energy of nuclear particles[1–5] or solar photons[6,7] to electric current have been investigated. However, conventional two-dimensional (2D) planar diode structures exhibit a number of inherent deficiencies that result in relatively low energy-conversion efficiencies. A unique three-dimensional (3D) porous silicon p–n diode has been developed to form the basis of a novel betavoltaic battery. Using tritium to demonstrate the proof-of-concept, the 3D diode geometry demonstrated a tenfold enhancement of efficiency compared to that of the usual 2D betavoltaic device geometry. Given the similarity of the energy-conversion physics for betavoltaic and photovoltaic devices, significant efficiency gains due to this 3D geometry might be expected for many types of photo detectors and solar cells.

The 3D diode was constructed on porous silicon (PS), which consists of a network of pores formed by electrochemical anodization of silicon substrates. According to the pore size, PS is classified as microporous (≤2 nm), mesoporous (2–50 nm), or macroporous (>50 nm). Such porous morphologies define a very large internal surface area,[8,9] which retains most of the characteristics associated with planar surface geometries, particularly for macropores.[10,11] Numerous investigations have been done on the physical and chemical properties of this complex material.[8,9,12] Moreover, it has been demonstrated that PS components can be integrated into microelectronic circuits in order to construct practical devices.[13] To date, however, PS has only been used as an antireflection and surface-passivation layer[14,15] in photovoltaic devices. It is believed that this work reports the first construction of conformal p–n junctions in PS.

PS diodes with a 3D p–n junction structure were created as illustrated schematically in Figure 1 (see Experimental for details). The continuous p–n junction can be visualized as a 2D "sheet" that is deformed to produce a uniform p–n junction layer on every accessible surface of the pore space. The built-in voltage[16] of the diodes was estimated to be ~0.8 V, assuming an n-dopant concentration of $\sim 5 \times 10^{18}$ cm^{-3} and an abrupt p–n junction doping profile. The metallurgical junction was about 200 nm below the surface, and the estimated depletion width on the p-side of the junction was ~1.4 μm.

The efficacy of the pore anodization procedure was investigated by means of scanning electron microscopy (SEM). Representative views of the top porous surface on the PS wafer

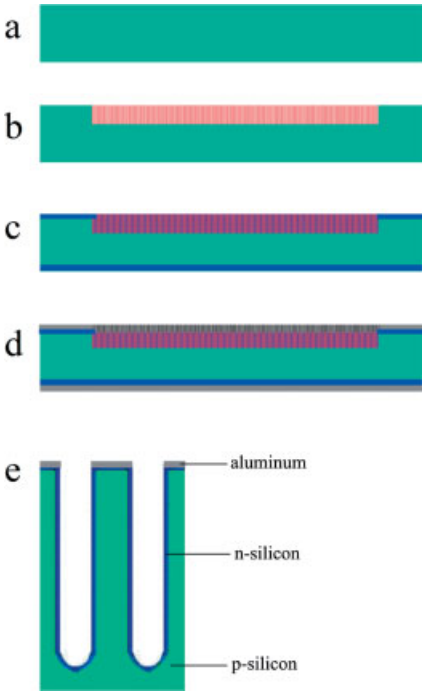

Figure 1. Fabrication procedure for the 3D porous silicon diode. a) Silicon wafer substrate. b) Macropores formed by electrochemical etching. c) p–n junctions introduced on all surfaces by solid-source diffusion. d) Aluminum ohmic contacts constructed on both sides. e) Representation of the continuous p–n junction in two neighboring pores.

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and the side view of a cleaved section are shown in Figures 2a,b, respectively. The pore throats are randomly distributed on the silicon surface. The pore channels shown in the side view are reasonably cylindrical with distinct small-scale variability along the pore walls.

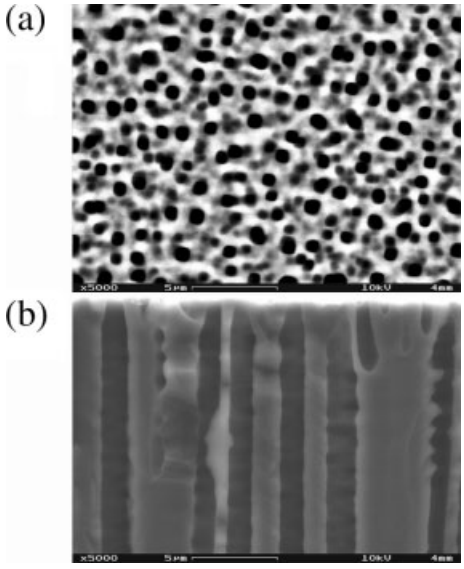

Figure 2. Geometry and morphology of the 3D porous diode. a) SEM image (top view). b) SEM image (cross-section).

In order to characterize the diode performance and to validate the diode fabrication procedures, standard techniques were used to obtain current–voltage (*I–V*) data for several planar and porous Si chips. Representative results are shown in Figure 3 for a planar diode and a porous diode. These diodes were from the same Si wafer as those exposed to tritium. Each Si diode under test was mounted "bare" in an integrated-circuit test box with the aluminum back-side pressed against a gold-plated flat surface by vacuum, and a tungsten needle contacting the front aluminum layer. The p–n junction characteristics shown in Figure 3a demonstrate that the porous diode behavior was comparable to that of the planar diode.

A marked photoresponse was observed for the porous diodes (Fig. 3b). The "dark" *I–V* curve is an expanded version of the PS diode data presented in Figure 3a. The "room light" curve (< 1 mW cm^{-2}) corresponds to fluorescent room lighting with the lid of the test box open, while the "bright light" (~ 10 mW cm^{-2}) data was obtained using the illumination lamp of a microscope held at a distance of ~ 3 cm. The planar diodes showed no photoresponse. This observation was attributed to the 50 nm thick Al contact covering the p–n junctions. Since such an Al contact also covered the p–n junction formed on the planar surface of the porous diode, the photovoltaic response appears to be entirely due to light entering the pores.

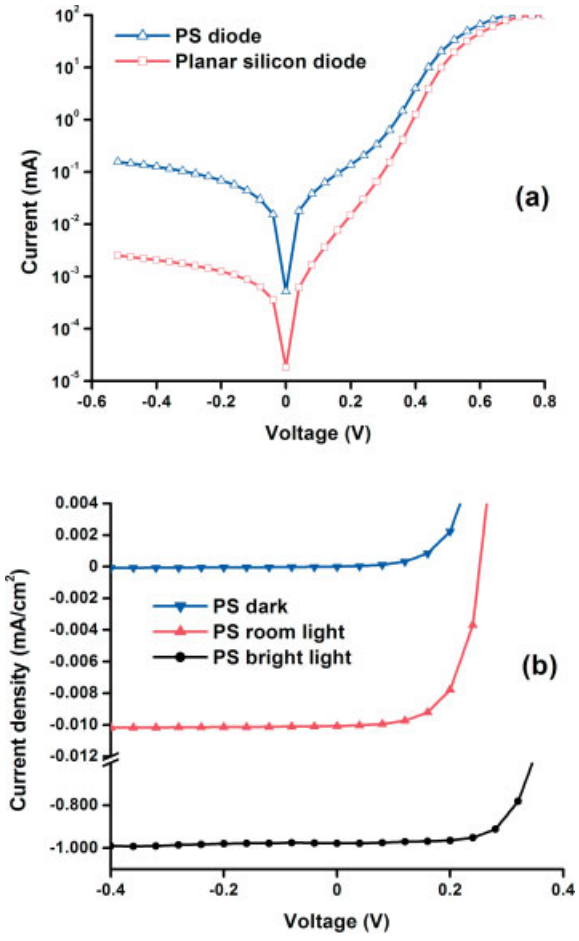

Figure 3. *I–V* characteristics measured at room temperature: a) porous and planar diodes show the same dark *I–V* characteristics with an ideality factor of 1.6 and 1.2, respectively. b) Photovoltaic effect under illumination in the porous diode. Estimated bright and room light intensities are ~ 10 mW cm^{-2} and < 1 mW cm^{-2}, respectively.

Preliminary investigation of the photovoltaic characteristics of initial 3D p–n diode samples with calibrated light sources was performed with the assistance of the National Renewable Energy Laboratory (NREL). *I–V* measurements were carried out using a Spectrolab X-25 solar simulator and its intensity was set with a primary reference cell and a spectral correction factor to simulate the global reference spectrum (IEC 60904). An overall power-conversion efficiency of 2.5 % was obtained from the measurements. As noted above, only the pore channels of the 3D diode contributed to the photoresponse. Combining the observation that the pores occupied 31 % of the available surface area with the results from the NREL, gives a photovoltaic power-conversion efficiency in the pore channels of 8 %. It is not unreasonable to expect that geometry modifications and improvements in diode performance can result in photoconversion efficiencies more than twice this value.

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The primary thrust of the research reported in this communication was to demonstrate the capability of 3D PS p–n diodes as betavoltaic energy storage and conversion devices. Tritium (^{3}H), an isotope of hydrogen with a half-life of 12.3 years, was chosen as the energy source. Gaseous tritium is the most benign radioactive material known, and has a low toxicity. The energetic electrons (beta particles) emitted when tritium nuclei decay have a spectrum of energies, with an average value of 5.69 keV and a maximum value of 18.6 keV. The corresponding average diffusion range in silicon is 0.79 μm, with a maximum of 4.3 μm. The estimated depletion depth of 1.4 μm is greater than the range of 84 % of the incident betas (corresponding to energy, $E_\beta \leq 9.3$ keV). Hence, the majority of the electron–hole pairs created were separated by drift. Further, given the large diffusion length of electrons in the low-doped p-type silicon, the remaining electron–hole pairs separated by diffusion.

Wafer test fixtures (WTFs) were designed and constructed to contain the tritium gas safely, and to simultaneously allow the Si diodes to be electrically isolated for testing before and after being loaded with tritium (see Supporting Information). Analysis of the pore geometry, together with the area enclosed by the indium seal in each WTF, gave the estimated number of pores exposed to tritium as 103 million. The corresponding total internal surface area was 116 cm^2 and the pore volume was 2.43×10^{-3} cm^3. The fraction of the surface containing pores was 0.31 and the remaining planar-surface fraction was 0.69.

Representative *I–V* responses for a 3D porous diode and a 2D planar diode, each installed within a WTF, are shown in Figure 4 before and after loading with tritium gas. The "knee", apparent in Figure 3 for the "bare" samples, is less evident in Figure 4 due to resistive effects and the low ratio of β-generation to reverse saturation-current densities in the WTFs. However, the presence of a built-in field does displace the *I–V* response curve into the fourth quadrant upon tritium exposure, indicating the generation of electrical power.

The increased efficiency resulting from the 3D porous diode structure may be more easily appreciated by scaling the tritium *I–V* curves with respect to unit radioactivity, as shown in Figure 4c. It is apparent that the short-circuit current ($V = 0$) per Curie of tritium is more than an order of magnitude greater for the 3D diode compared to the conventional 2D diode geometry. The reproducibility of the data shown in Figure 4c was confirmed by using different equipment in two independent laboratories (see Supporting Information).

The physical principles of operation for both betavoltaic and photovoltaic devices are very similar other than in the source of energy and generation of excess carriers. The data and the analysis procedures used to evaluate the performance of the 2D planar and 3D porous betavoltaic diodes are described in the accompanying Supporting Information.

The average observed efficiencies were $\eta_{2D} = 0.023$ % and $\eta_{3D} = 0.22$ % for the planar diode and for the pore channels of the porous diode, respectively. These rather low values are mostly attributed to the correspondingly low power available from the small volumes of tritium gas. However, it is interesting to observe that the ratio of the energy-conversion efficiencies for the 3D porous to 2D planar devices is $\eta_{3D}/\eta_{2D} = 9.9 \pm 2.2$.

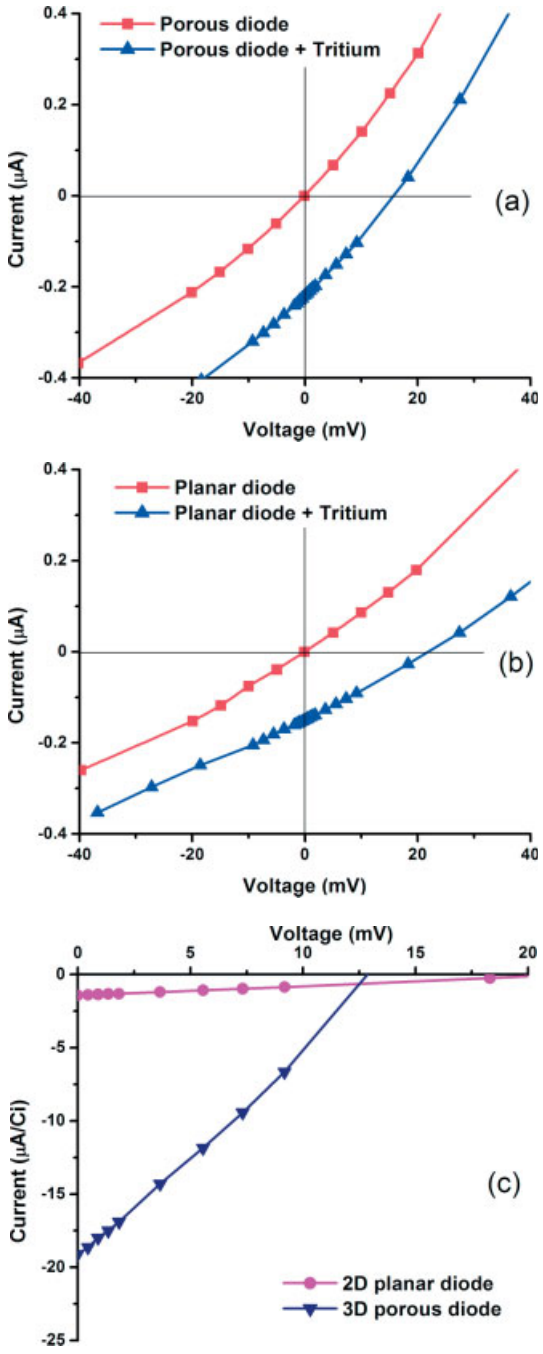

Figure 4. *I–V* characteristics measured with diodes in the WTFs: a) porous diode before and after tritium loading; b) planar diode before and after tritium loading. c) Current per unit radioactivity, showing enhancement for the 3D porous geometry device compared to the usual 2D planar device.

This order-of-magnitude increase in efficiency in the pore channels corresponds to the almost unity probability that tritium-decay electrons enter the betavoltaic conversion layers (i.e., the p–n junctions) on the pore walls. This follows for three major reasons: First, no matter what the direction of flight, and considering that the length/diameter ratio of the pores is ~60:1, the average path length prior to striking the pore walls is less than 2 μm. Next, there is negligible self-absorption in the tritium gas within the pore channels (~1 μm diameter). Finally, although it is estimated that ~1/3 of the incident betas may be elastically backscattered,[2] the fraction lost is nearly zero in the pores due to the close proximity of "adjacent" betavoltaic junctions.

A supporting solid-angle argument is made as follows: Suppose that the solid-angle ratio is the same as the efficiency ratio ($\Omega_{3D}/\Omega_{2D} = 9.9$), and also assume that $\Omega_{3D} = 4\pi$ sr (steradian), then $\Omega_{2D} = 1.27$ sr. Including the backscattering losses noted above increases the effective solid angle to $\Omega_{2D} \approx 1.9$ sr. Clearly, the effective solid angle for a "disk" of tritium above a planar surface is in the range of π to $\pi/2$ sr, which brackets the above value.

In summary, we have demonstrated that a 3D PS diode structure can be constructed using standard fabrication techniques used in the semiconductor industry. This geometry increases the betavoltaic power-generation efficiency by a factor of ten compared to that of planar diode devices. This result suggests that almost every energetic electron emitted as a result of tritium decay enters a nearby betavoltaic junction. It is expected that an increase in the radioisotope energy density in the pores using high-density tritiated compounds along with improvements in device quality will yield a far more efficient, long-life betavoltaic device. In addition, quantitative evaluation of the photovoltaic response of 3D porous diodes suggests that this geometry will provide significant benefits for photodetectors, solar cells, and other devices for which light–semiconductor interactions are important.

Experimental

Porous Silicon Fabrication: Boron-doped p<100> silicon wafers (550 μm thick with a resistivity of 20–30 Ω cm) were used as the substrates (Fig. 1a). Porous silicon (PS) was prepared using an anodization process in a custom-designed single etching cell. A tungsten mesh was used as the cathode while the anode was an aluminum sheet pressed against the back-side of the wafer. An electrolyte of 4 wt.-% hydrofluoric acid (HF) in dimethylformamide (DMF) was freshly made for the anodization. The silicon wafer was first dipped into buffered oxide etchant (BOE) to strip the natural oxide on the surface. Then, the wafer was etched in the cell with a current density of 2 mA cm^{-2} for 180 min to produce a PS layer thickness of 40–50 μm (Fig. 1b). Finally, standard RCA cleaning was carried out to eliminate metal and organic species that could cause contamination in later steps.

p–n Junction Construction: A continuous p–n junction was formed on the external and internal surfaces of each PS layer. The same procedure was used to produce p–n junctions on the planar surfaces of Si wafers, which were used for comparison purposes. Phosphorus, an n-type dopant, was introduced into the pores of the p-type silicon matrix by solid-source diffusion (Fig. 1c). Each Si wafer was soaked in a tube furnace for 9 min to make a shallow n^+ layer (~200 nm thick) on the planar surface and inside the pore channels. Afterwards, the n^+ layer that formed on the back-side of the Si wafer was removed by SF_6-plasma dry etching. Then the wafers were dipped into BOE to strip off the SiO_2, so that a good ohmic contact could be constructed on the bare Si surface. The wafers were immediately placed in a high vacuum chamber ($< 10^{-7}$ torr or $\approx 133 \times 10^{-7}$ Pa) for the evaporation of Al–Si alloy (2 % Si). Al layers 50 nm and 200 nm thick were formed on the porous side and back-side, respectively. To avoid a Schottky barrier at the interface of the aluminum and silicon, the samples were annealed at 420 °C for 15 min (Fig. 1d). The wafers were cleaved into 2.54 cm × 2.54 cm squares and rinsed with acetone, isopropyl alcohol, and de-ionized water.

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Supplementary Materials

A Three Dimensional Porous Silicon p-n Diode for Betavoltaics and Photovoltaics

Pore Parameter Analysis: The morphology of selected macroporous Si samples was observed in detail with a scanning electron microscope (SEM). Figure 2 presents a top view (a) and a side view of a cleaved Si chip (b) showing representative pore channel cross sections. The SEM data were used to estimate the geometrical parameters of the randomly distributed pores. The area of the SEM view was 337.5 μm^2. A manual count showed 135 well-focused pore openings and 55 blurred openings giving a total of 190 pores. This gives the average surface area containing each pore as 1.78 μm^2. A selection of 50 pores in this area gave the average pore diameter, d_{avg}, as 0.84 ± 0.12 μm. A total of 17 pore channels were randomly selected from the SEM cross section view to estimate the average pore depth, h_{avg}, as 43.1 ± 1.2 μm.

Wafer Test Fixture: Both porous silicon and planar silicon *p-n* diodes were exposed to tritium within the confines of Wafer Test Fixtures (WTFs). Each WTF consisted of two steel plates 6.35 cm in diameter bolted together and tightly clamping a 1.91 cm diameter copper disc (silver soldered to a 0.32 cm diameter copper fill pipe), a 0.1 cm diameter indium wire seal ring, and a 2.54 cm × 2.54 cm square Si wafer. The indium wire seal was a 1.52 cm diameter circle that compressed to a thickness of ~0.02 cm when the assembly was completely sealed.

PEEK insulators placed between the top and bottom plates and the central components provided electrical isolation. An electrical conductor, entering via a hole in the bottom plate, was attached to the backside of the Si wafer with silver epoxy. The other end of the conductor was soldered to a BNC bulkhead feedthrough mounted on a standoff connected to the bottom plate. The *p-n* junctions on the front-side of the Si wafer faced the fill pipe. The circuit to the measurement equipment was completed by an electrical conductor clipped to the fill pipe.

Each assembled WTF was installed on a high vacuum system and standard techniques used to confirm vacuum leak tightness of less than 10^{-8} atm·cm^3/s. Thereafter, 232 mCi of tritium gas at a pressure slightly above 1 atm was loaded into each WTF. The WTFs were separated from the Tritium Handling System by cold-weld pinching of the Cu fill pipe at the mid point. Wipe tests following loading and subsequent measurement operations verified minimal residual contamination. Accepted radioactive handling procedures were used when handling, shipping and storing the WTFs containing tritium.

Efficiency Analysis: The analysis of the *I-V* data followed established methods to determine the device performance. The energy conversion efficiency, η, given by the following expression:

$$\eta = P_{ex} * FF / P_{\beta} \quad (1)$$

where P_{β} is the volumetric power produced by the radioisotope and P_{ex} is the product of the short circuit current and the open circuit voltage. The fill factor is given by:

$$FF = P_{m4} / P_{ex} \quad (2)$$

where P_{m4} is the maximum "power rectangle" in the 4th quadrant of the *I-V* response.

The available tritium beta power per unit radioactivity is P_{β} = 33.7 μW per curie (Ci). In the WTFs, there was 106 mCi of tritium activity above the Si diodes and the pore channels contained 6.04 mCi. Note that it is common practice to define P_{β} per unit area for betavoltaic power.[2] However, in this work P_{β} is the total available power contained in the reservoir volume. The main point of interest is how much of the complete solid angle of 4π steradians contributes to the energy conversion process in the pore channels, and thus the potential utilization of the available power.

The tritium power parameters extracted from two *I-V* response data sets are presented in Table 1. WTF1 contained a 3D porous diode and WTF2, a 2D planar diode. The notation, "both" for WTF1 refers to the fact that the *p-n* junction for the porous diode was fabricated both on the planar surface and on the walls of the pore channels. Since the pore openings occupied 31% of the planar surface area of the porous diode, the power developed in the pore channels, "P in pores," was estimated with the relation, $P_p = P_1 - 0.69*P_2$, and similarly the pore current, "I in pores," via $I_p = I_1 - 0.69* I_2$. The subscripts 1 and 2 denote the porous diode WTF1 and planar diode WTF2, respectively.

Table S1. Tritium power and efficiency parameters from I-V data analysis.

Location *(Investigator)*	*WTF(Contents)*	I_{sc} *(nA)*	V_{oc} *(mV)*	P_{ex} *(nW)*	*FF*	P_β (μW)	η	η_{3D}/η_{2D}
Houston (Gadeken)	2(planar)	150	22.8	3.41	0.26	3.57	0.249×10^{-3}	
	1(both)†	219	17.3	3.78	0.26			
	1(P in pores)†			1.43		0.203	1.92×10^{-3}	7.7
	1(I in pores)†	116	13.2	1.53	0.27	0.203	2.05×10^{-3}	8.3
Toronto (Kherani)	2(planar)	145	15.6	2.25	0.33	3.57	0.206×10^{-3}	
	1(both)†	236	13.1	3.09	0.32			
	1(P in pores)†			1.54		0.203	2.40×10^{-3}	11.6
	1(I in pores)†	139	13.7	1.91	0.26	0.203	2.45×10^{-3}	11.9

†See text for nomenclature.